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Simics: A full system simulation platform

PI Magnusson H Christensson J Eriksson D ... - COMPUFUTEP, 2002 - [portal.acm.org](#)
 ... Naturally, we wish to **simulate** an entire system and to do so with total accuracy—a perfect ... Simics is also sufficiently **generic** to **model** embedded systems, desktop or set-top boxes, telecom ... Simics simulates processors at the **instruction set** level, including the full supervisor state ...
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LISA—machine description language for cycle-accurate models of programmable DSP architectures[psu.edu](#) [PDF]

S Pees A Hoffmann V Zingovici, H ... - Proceedings of the 36th ... 1999 - [portal.acm.org](#)
 ... HDLs like VHDL or Verilog are widely used to **model** and **simulate** processors, but ... Texas Instruments, TMS320C6x/C67x CPU and In-struction Set Reference Guide, Mar ... D. Bradles, R. Henry, and S. Eggers, "The Marlin system for reconfigurable **instruction scheduling**," in Proc ...
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[PDF] Generation of interpretive and compiled instruction set simulators[psu.edu](#) [PDF]

R Leupen, J Fiste, B Landwehr - Proceedings of the ASP-DAC, 1999 - Citeseer
 ... or PC host, such tools have to be designed as cross-compilers or cross-simulators, respectively, which generate and **simulate** code for ... The Insulin **instruction-set** simulator is part of the FlexWare system 5. It is based on a configurable VHDL model of a "generic" processor ...
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A universal technique for fast and flexible instruction-set architecture simulation[psu.edu](#) [PDF]

A Nigh, G Braun, O Schiebisch, R Leupen, ... - Proceedings of the ... 2002 - [portal.acm.org](#)
 ... and sequences the appropriate host operations that are required to **simulate** the application ... A **LISA model** is a mixed structural/behavioral description of a process ... The process- or **instruction-set** including **instruction-coding**, assembly syntax, functional behavior, and timing ...
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A novel methodology for the design of application-specific instruction-set processors (ASIPs) using a machine description language[psu.edu](#) [PDF]

A Hoffmann, J Kogel, A Vogt, S Braun, ... - on computer-aided ... 2001 - [leeeuplate.lee.org](#)
 ... HDLs like VHDL or Verilog are widely used to **model** and **simulate** processors, but ... Considering **instruction-set** simulation, efficient runtime reduction can be achieved by per- forming repeatedly ... tion-accurate **models**, it becomes a complex task for **models** with **instruction pipelines** ...
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Hardware/software instruction set configurability for system-on-chip processors[psu.edu](#) [PDF]

A Wang, E Klein, D Maydan, G ... - Proceedings of the 36th ... 2001 - [portal.acm.org](#)
 ... The simulator is able to correctly **simulate** an Xlens program at close to one million instructions per second regardless of whether the simulated program uses TIE ... "ISDL: An **instruction set** description language ... "LISA - machine description language and **generic** machine **model** ...
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Asim: A performance model framework[psu.edu](#) [PDF]

J Ermer P Abuzo E Borch, A Fausser, CK Luk, G ... - Computer, 2002 - [leeeuplate.lee.org](#)
 ... The Aint feeder, the most aggressive in this set of **instruction feeders**, 2 supplies ... Aint fetches and executes any **instruction** under the direction of the performance **model**, but ... Aint can help a performance **model** correctly **simulate** a modern, dynamically scheduled, speculative micro ...
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The M5 simulator: Modeling networked systems

NL Binkov, RG Drasinski, LK Haus, KT Lim, AG ... - IEEE ... 2006 - [leeeuplate.lee.org](#)
 ... Using this language, a simple add **instruction** could be coded as Rc = Ra + Rb. A parser converts the ISA description to a set of **instruction classes**, which include methods that ... of warm-up time required for TCP to stabilize can be significantly larger than is practical to **simulate** ...
[Cited by 268](#) - [Related articles](#) - [All 26 citations](#)

A generic tool set for application specific processor architectures[psu.edu](#) [PDF]

F Engel, J Nührenberg, GP Fettweis - Proceedings of the eighth ... 2000 - [portal.acm.org](#)
 ... During simulation a jump to the succeeding **instruction** sequence is necessary ... As part of the M5-DSP chip **set** this processor is responsible for pre- and post-processing ... Hence to **simulate** correct response times a cycle accurate **model** with full control of the pipeline behavior is ...
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Automatic generation of fast timed simulation models for operating systems in SoC design[psu.edu](#) [PDF]

S Yoo, G Nouraei, t Gummer, A ... - Proceedings of the ... 2002 - [portal.acm.org](#)
 ... SoC OS also enables to **model** final OSs with a **generic** OS simulation **model** [15], ... OS, the designer needs to run more accurate simulation such as using **instruction set** simulators ... To **simulate** a specific OS implementation, the designer needs to do "personalization" of the virtual ...
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